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10/743,793	12/24/2003	Katsuto Tanahashi	032206	9788

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EXAMINER
KIM, JAY C

ART UNIT	PAPER NUMBER
2815	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/743,793	TANAHASHI ET AL.	
	Examiner	Art Unit	
	JAY C. KIM	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 July 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 4-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 4-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the Amendment filed July 18, 2008.

Claim Objections

1. Claim 1 is objected to because of the following informalities: on the last line, "(atoms/cm^3)or higher" should be replaced by "(atoms/cm^3) or higher". Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1 and 4-12 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claims contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention. Regarding claim 1, Applicants disclose that "the carbon concentration is defined to be 1×10^{15} (atoms/cm^3) or higher" in the Specification. Therefore, one of ordinary skill in the art would recognize that *a carbon concentration* is 1×10^{15} (atoms/cm^3) or higher in the semiconductor substrate, not that a carbon concentration is uniformly 1×10^{15} (atoms/cm^3) or higher. Claims 4-12 depend

on claim 1, and therefore claims 4-12 also fail to comply with the written description requirement.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1 and 4-12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Regarding claim 1, it is not clear what "the whole area of the depth direction" refers to, because a depth direction cannot have an area. Claims 4-12 depend on claim 1, and therefore claims 4-12 are also indefinite. In the below prior art rejections, it is interpreted that "the whole area of the depth direction" refers to a whole in-plane area at a depth.

6. Claim 1 recites the limitations "the whole area" and "the depth direction" in a semiconductor substrate. There are insufficient antecedent bases for these limitations in the claim. Claims 4-12 depend on claim 1, and therefore claims 4-12 are also indefinite.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1, 4, 5 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Asayama et al. (US 6,365,461) in view of Wenski et al. (US 6,458,688) and further in view of Takizawa et al. (US 5,734,195) and then further in view of Ishida et al. (US 6,198,157).

Regarding claims 1 and 4, Asayama et al. disclose a semiconductor substrate (col. 9, lines 43-45) containing boron at a concentration of 1×10^{17} (atoms/cm^3).

Asayama et al. differ from the claimed invention by not comprising a front face and a rear face that are both mirror-polished, wherein the semiconductor substrate meets an SFQR value ≤ 70 (nm) as a flatness of the front face, wherein a crystal layer is provided on the front face, wherein a minimum value of the concentration of boron [B] (atoms/cm^3) is defined for a required thickness t (μm) of the crystal layer within the range of the concentration of boron, based on a relational equation $[B] \geq (2.2 \pm 0.2) \times 10^{16} \exp(0.21t)$, and wherein the semiconductor substrate contains carbon at a concentration of 1×10^{15} (atoms/cm^3) or higher across a whole in-plane area at a depth (claim 1), wherein a maximum value of a thickness t (μm) of the crystal layer is defined for a required concentration of boron [B] (atoms/cm^3), based on a relational equation $[B] \geq (2.2 \pm 0.2) \times 10^{16} \exp(0.21t)$ (claim 4).

Wenski et al. disclose a semiconductor substrate (Fig. 1) comprising a front face and a rear face that are both mirror-polished (col. 7, lines 42-43), wherein the

semiconductor substrate (Fig. 1) meets an SFQR value ≤ 70 (nm) or 0.07 μm (Please note that the numbers in Fig. 1 are in μm, because a maximum SFQR value is less than or equal to 0.13 μm (lines 3-5 of ABSTRACT).) as a flatness of the front face.

Since both Asayama et al. and Wenski et al. teach a semiconductor substrate, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor substrate disclosed by Asayama et al. with the double-side polished semiconductor substrate disclosed by Wenski et al., because double-side polishing is well-known in manufacturing a semiconductor substrate to reduce surface roughness of the semiconductor substrate to improve the yield of the semiconductor devices formed on the semiconductor substrate.

Further regarding claims 1 and 4, Asayama et al. in view of Wenski et al. differ from the claimed invention by not showing that a crystal layer is provided on the front face, wherein a minimum value of the concentration of boron [B] (atoms/cm^3) is defined for a required thickness t (μm) of the crystal layer within the range of the concentration of boron, based on a relational equation $[B] \geq (2.2 \pm 0.2) \times 10^{16} \exp(0.21t)$, and wherein the semiconductor substrate contains carbon at a concentration of 1×10^{15} (atoms/cm^3) or higher across a whole in-plane area at a depth (claim 1), wherein a maximum value of a thickness t (μm) of the crystal layer is defined for a required concentration of boron [B] (atoms/cm^3), based on a relational equation $[B] \geq (2.2 \pm 0.2) \times 10^{16} \exp(0.21t)$ (claim 4).

Takizawa et al. disclose a semiconductor substrate (composite layer of 11 and 15 in Fig. 3C) (col. 4, lines 22-23 and 41) comprising a front face (12) that is mirror-

polished (col. 4, lines 24-25), wherein a crystal layer (16) (col. 4, lines 47-49) is provided on the front face (12), wherein the thickness t (μm) of the crystal layer (16) is about 10 μm, and wherein the semiconductor substrate (composite layer of 11 and 15) contains carbon (15) at a concentration of 1×10^{16} (atoms/cm^3) or higher across a whole in-plane area at a depth (col. 4, lines 43-45).

Since both Asayama et al. and Takizawa et al. teach a semiconductor substrate containing oxygen, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor substrate disclosed by Asayama et al. in view of Wenski et al. with the carbon implanted region disclosed by Takizawa et al., because the carbon implanted region would accelerate oxygen precipitation to improve gettering of impurities in the semiconductor substrate (Takizawa et al., col. 2, lines 23-27).

Further regarding claims 1 and 4, Asayama et al. in view of Wenski et al. and further in view of Takizawa et al. differ from the claimed invention by not showing that a minimum value of the concentration of boron [B] (atoms/cm^3) is defined for a required thickness t (μm) of the crystal layer within the range of the concentration of boron, based on a relational equation $[B] \geq (2.2 \pm 0.2) \times 10^{16} \exp(0.21t)$ (claim 1), and wherein a maximum value of a thickness t (μm) of the crystal layer is defined for a required concentration of boron [B] (atoms/cm^3), based on a relational equation $[B] > (2.2 \pm 0.2) \times 10^{16} \exp(0.21t)$ (claim 4).

Ishida et al. disclose a semiconductor substrate (101 in Fig. 1c), wherein a crystal layer (102) is provided on the front surface and about 5 μm thick (col. 6, lines 46-

49), which would satisfy the relational equation of a minimum value of the concentration of boron [B] (atoms/cm^3) and a required thickness t (μm) of the crystal layer $[B] \geq (2.2 \pm 0.2) \times 10^{16} \exp(0.21t)$, which suggests $t \leq 7.7$ μm when $[B] = 1 \times 10^{17}$ (atoms/cm^3), and therefore a maximum value of a thickness t (μm) of the crystal layer disclosed by Asayama et al. in view of Wenski et al. and further in view of Takizawa et al. and then further in view of Ishida et al. is defined for a required concentration of boron $[B] = 1 \times 10^{17}$ (atoms/cm^3), based on a relational equation $[B] \geq (2.2 \pm 0.2) \times 10^{16} \exp(0.21t)$, which suggests $t \leq 7.7$ μm when $[B] = 1 \times 10^{17}$ (atoms/cm^3).

Since both Asayama et al. and Ishida et al. teach a crystal layer formed on a semiconductor substrate, it would have been obvious to the one of ordinary skill in the art at the time the invention was made that the thickness of the crystal layer disclosed by Asayama et al. in view of Wenski et al. and further in view of Takizawa et al. may be about 5 μm as disclosed by Ishida et al., because the thickness of the crystal layer can be varied depending on the products and manufacturing conditions of the semiconductor device formed on the semiconductor substrate (Ishida et al., col. 6, lines 46-48).

Regarding claim 5, Takizawa et al. further disclose that the crystal layer (16) is a silicon crystal layer formed by epitaxial growth (col. 4, line 47).

Regarding claim 12, Asayama et al. in view of Wenski et al. and further in view of Takizawa et al. and then further in view of Ishida et al. disclose the semiconductor substrate according to claim 1.

The claim limitation "the rear face is in an exposed state, or a natural oxide film having a thickness of 1 (nm) or less is formed on the rear face" specifies an intended use or field of use, because, for example, if the semiconductor substrate is kept in vacuum, no natural oxide film would be formed on the rear face, and is treated as non-limiting since it has been held that in device claims, intended use must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. *In re Casey*, 152 USPQ 235 (CCPA 1967); *In re Otto*, 136 USPQ 458, 459 (CCPA 1963). A claim containing a "recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus" if the prior art apparatus teaches all the structural limitations of the claim. *Ex Parte Masham*, 2 USPQ 2d 1647 (Bd. Pat. App. & Inter. 1987).

9. Claims 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Asayama et al. (US 6,365,461) in view of Wenski et al. (US 6,458,688) and further in view of Takizawa et al. (US 5,734,195) and then further in view of Ishida et al. (US 6,198,157) as applied to claim 1 above, and then further modified by Fitzgerald (US 2002/0123167). The teachings of Asayama et al. in view of Wenski et al. and further in view of Takizawa et al. and then further in view of Ishida et al. are discussed above.

Regarding claim 6, Asayama et al. in view of Wenski et al. and further in view of Takizawa et al. and then further in view of Ishida et al. differ from the claimed invention by not showing that the crystal layer is a silicon-germanium alloy crystal layer.

Fitzgerald discloses a semiconductor substrate (102 in Fig. 1), wherein a silicon-germanium alloy crystal layer (composite layer of 104 and 106) is provided on the front face.

Since both Asayama et al. and Fitzgerald teach a semiconductor substrate, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor substrate disclosed by Asayama et al. in view of Wenski et al. and further in view of Takizawa et al. and then further in view of Ishida et al. with the silicon-germanium alloy crystal layer disclosed by Fitzgerald, because forming a silicon-germanium alloy crystal layer on a silicon substrate is well-known in manufacturing a semiconductor device to apply strain on a channel layer that will be formed on the silicon-germanium alloy crystal layer.

Regarding claim 7, Asayama et al. in view of Wenski et al. and further in view of Takizawa et al. and then further in view of Ishida et al. differ from the claimed invention by not showing that the crystal layer is a layer in a layered structure of a silicon-germanium alloy crystal layer and a silicon crystal layer.

Fitzgerald discloses a semiconductor substrate (504 in Fig. 5D) (lines 5-9 of [0035]), wherein a layered structure (composite layer of 502 and 508) (line 17 of [0035]) of a silicon-germanium alloy crystal layer (502) and a silicon crystal layer (508) is provided on the front face of the substrate (504).

Since both Asayama et al. and Fitzgerald teach a semiconductor substrate, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor substrate disclosed by Asayama et al. in view of Wenski et al. and further in view of Takizawa et al. and then further in view of Ishida et al. with the layered structure of a silicon-germanium alloy crystal layer and a silicon crystal layer disclosed by Fitzgerald, because forming a layered structure of a silicon-germanium alloy crystal layer and a silicon crystal layer on a silicon substrate is well-known in manufacturing a semiconductor device to apply strain on the silicon layer that will be used as a channel layer.

Regarding claims 7 and 8, Asayama et al. in view of Wenski et al. and further in view of Takizawa et al. and then further in view of Ishida et al. differ from the claimed invention by not showing that the crystal layer is a layer in a layered structure of a silicon-germanium alloy crystal layer and a silicon crystal layer (claim 7), wherein the silicon crystal layer is formed in an SOI structure in which the silicon crystal layer is separated by a silicon oxide layer (claim 8).

Fitzgerald discloses a layered structure (800, 802 and 808 combined in Fig. 8B) (lines 1-2 and 6-7 of [0041]) of a silicon-germanium alloy crystal layer (800) and two silicon crystal layers (802 and 808), wherein the top silicon poly-crystal layer (808) is formed in an SOI structure in which the top silicon poly-crystal layer (808) is separated by a silicon oxide layer (806).

Since both Asayama et al. and Fitzgerald teach a semiconductor substrate, it would have been obvious to the one of ordinary skill in the art at the time the invention

was made to combine the semiconductor substrate disclosed by Asayama et al. in view of Wenski et al. and further in view of Takizawa et al. and then further in view of Ishida et al. with the layered structure of a silicon-germanium alloy crystal layer and two silicon crystal layers separated by a silicon oxide layer disclosed by Fitzgerald, because the top silicon poly-crystal layer and the silicon oxide layer would protect the strained silicon layer during semiconductor processing.

10. Claims 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Asayama et al. (US 6,365,461) in view of Wenski et al. (US 6,458,688) and further in view of Takizawa et al. (US 5,734,195) and then further in view of Ishida et al. (US 6,198,157) as applied to claim 1 above, and further modified by Inazuki et al. (US 6,362,076). The teachings of Asayama et al. in view of Wenski et al. and further in view of Takizawa et al. and then further in view of Ishida et al. are discussed above.

Regarding claims 9 and 11, Asayama et al. in view of Wenski et al. and further in view of Takizawa et al. and then further in view of Ishida et al. differ from the claimed invention by not showing that the semiconductor substrate is an SOI substrate, and wherein the crystal layer is an upper silicon crystal layer separated by a silicon oxide layer (claim 9), wherein the SOI substrate is formed by a bonding method (claim 11).

Inazuki et al. disclose a semiconductor substrate (6 in Fig. 1), which is an SOI substrate (col. 4, lines 48-50, and col. 5, line 6), and a crystal layer (7) (col. 5, lines 6-7) separated from the SOI substrate (6) by a silicon oxide layer (3) (col. 4, line 54), wherein the SOI substrate (6) is formed by a bonding method.

Since both Asayama et al. and Inazuki et al. teach a semiconductor substrate, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor substrate disclosed by Asayama et al. in view of Wenski et al. and further in view of Takizawa et al. and then further in view of Ishida et al. with the wafer bonding method disclosed by Inazuki et al., because the resulting structure can be used for forming a field effect transistor using the SOI channel layer to improve semiconductor device performance.

Regarding claim 10, Asayama et al. in view of Wenski et al. and further in view of Takizawa et al. and then further in view of Ishida et al. and further modified by Inazuki et al. disclose the semiconductor substrate according to claim 9.

The limitation that "the SOI substrate is formed by a SIMOX method" is a product-by-process limitation that does not structurally distinguish the claimed invention over the prior art. Note that a product by process claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wertheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and *In re Marosi et al*, 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a product by process claim, and not the patentability of the process, and that an old or obvious product by a new method is not patentable as a product, whether claimed in product by process claims or not. Note that applicant has the burden of proof in such

cases, as the above case law makes clear.

Response to Arguments

11. Applicants' arguments with respect to claim 1 have been considered but are moot in view of the new grounds of rejection under 35 U.S.C. 112, first paragraph and second paragraph.

Applicants argue that "the present invention of claim 1 and claims dependent therefrom contains carbon at a concentration equally across the whole area of the depth direction of semiconductor substrate". Applicants do not claim an equal carbon concentration. Also, a depth direction cannot have an area.

Conclusion

12. Applicants' amendment necessitated the new grounds of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicants are reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAY C. KIM whose telephone number is (571)270-1620. The examiner can normally be reached on 7:30 AM - 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jerome Jackson Jr./
Primary Examiner, Art Unit 2815

/J. K./
Examiner, Art Unit 2815
August 27, 2008